TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSII)

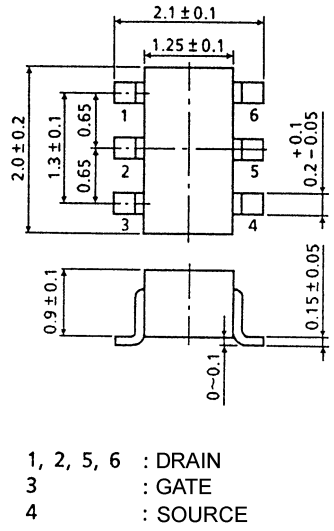
SSM6J08FU

Power Management Switch

DC-DC Converter

- Small Package
- Low on Resistance : R_{on} = 0.18 Ω (max) (@V_{GS} = −4 V)
  : R_{on} = 0.26 Ω (max) (@V_{GS} = −2.5 V)
- Low Gate Threshold Voltage

Unit: mm



1, 2, 5, 6 : DRAIN
3 : GATE
4 : SOURCE

US6

JEDEC	—
JEITA	—
TOSHIBA	2-2J1D

Weight: 6.8 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

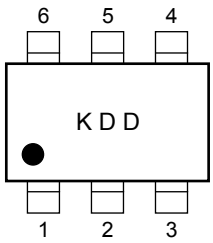
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	−20	V
Gate-Source voltage		V_{GSS}	±12	V
Drain current	DC	I_D	−1.3	A
	Pulse	I_{DP} (Note 2)	−2.6	
Drain power dissipation		P_D (Note 1)	300	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 mm^2 × 6) Fig: 1.

Note 2: The pulse width limited by max channel temperature.

Marking



Equivalent Circuit

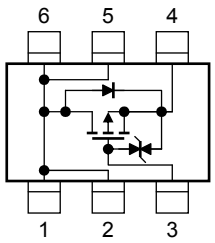
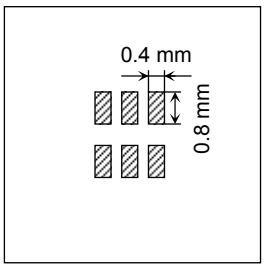


Fig 1: 25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 mm^2 × 6



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

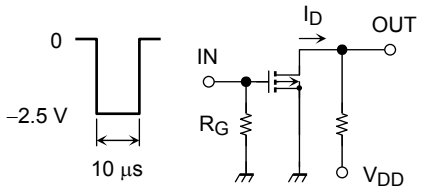
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−20	—	—	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = 12 V	−8	—	—	
Drain Cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	—	—	−1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −0.1 mA	−0.5	—	−1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −0.65 A (Note 3)	1.3	2.7	—	S
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = −0.65 A, V_{GS} = −4 V (Note 3)	—	140	180	mΩ
			I_D = −0.65 A, V_{GS} = −2.5 V (Note 3)	—	200	260	
			I_D = −0.65 A, V_{GS} = −2.0 V (Note 3)	—	260	460	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	370	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	73	—	pF
Output capacitance		C_{oss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	116	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.65 A,	—	33	—	ns
	Turn-off time	t_{off}	V_{GS} = 0~−2.5 V, R_G = 4.7 Ω	—	47	—	ns

Note 3: Pulse test

Switching Time Test Circuit

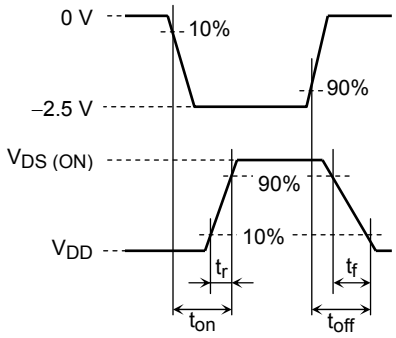
(a) Test circuit



V_{DD} = −10 V
R_G = 4.7 Ω
D.U. ≦ 1%
V_{IN}: t_r, t_f < 5 ns
COMMON SOURCE
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



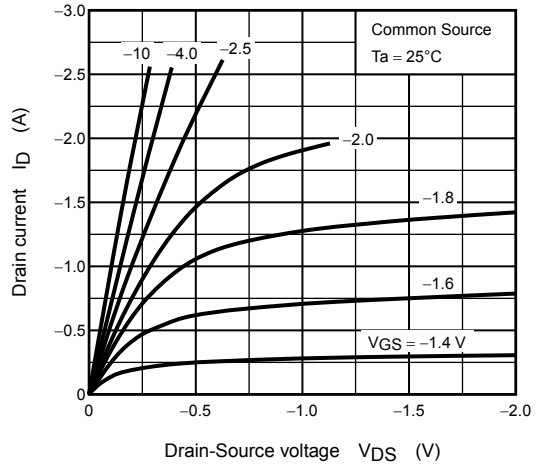
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = −100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}.

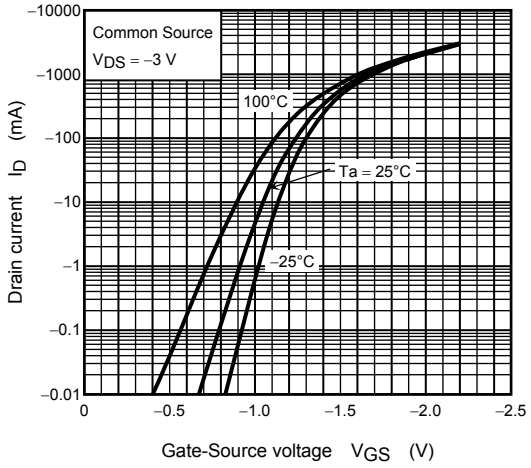
(relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

Please take this into consideration for using the device.

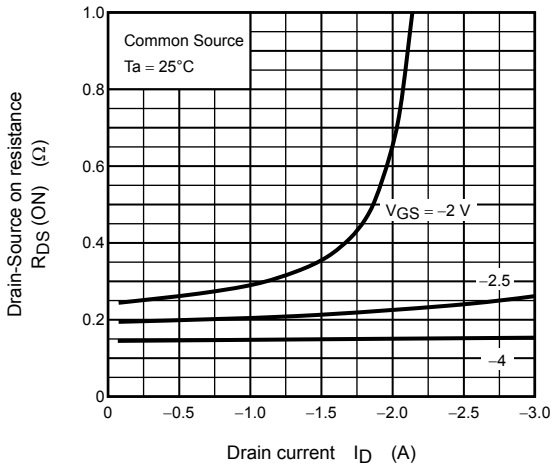
$I_D - V_{DS}$



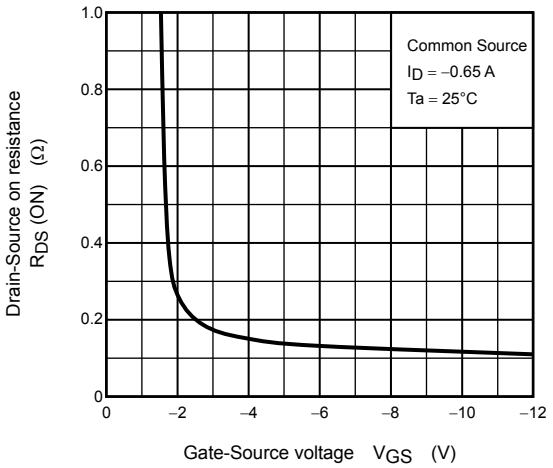
$I_D - V_{GS}$



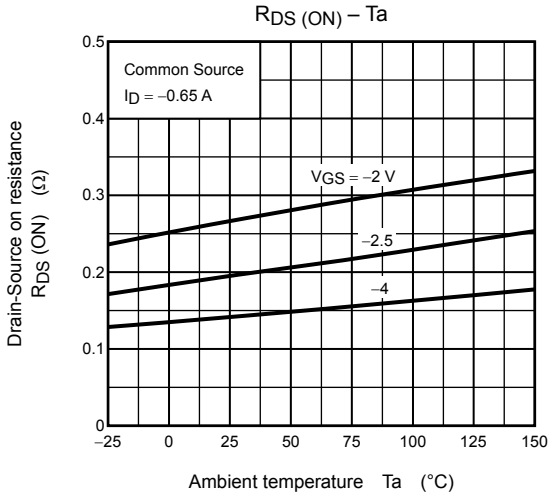
$R_{DS\ (ON)} - I_D$



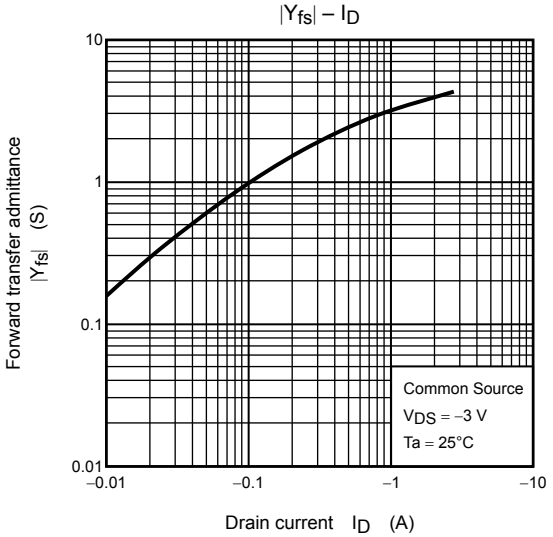
$R_{DS\ (ON)} - V_{GS}$



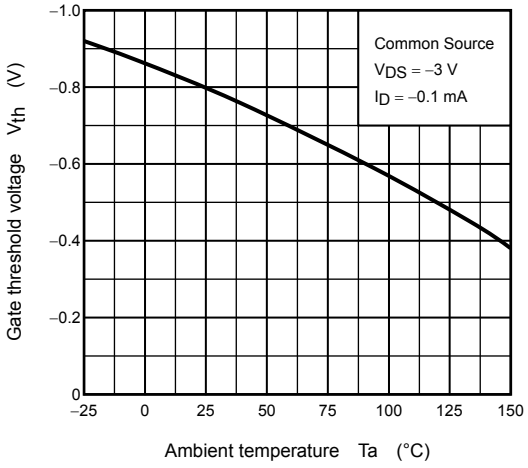
$R_{DS\ (ON)} - Ta$



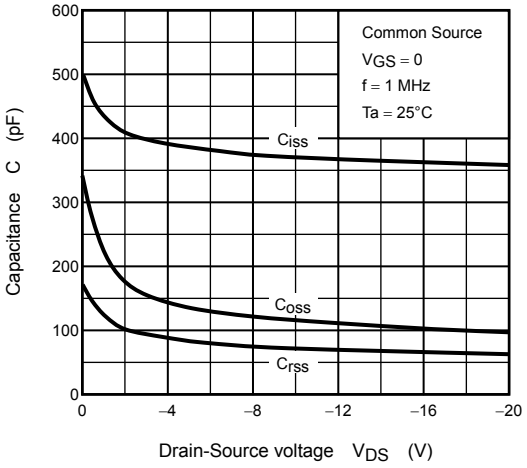
$|Y_{fs}| - I_D$



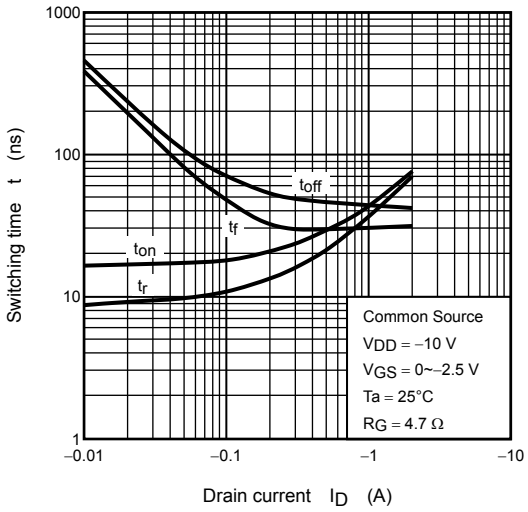
V_{th} – Ta



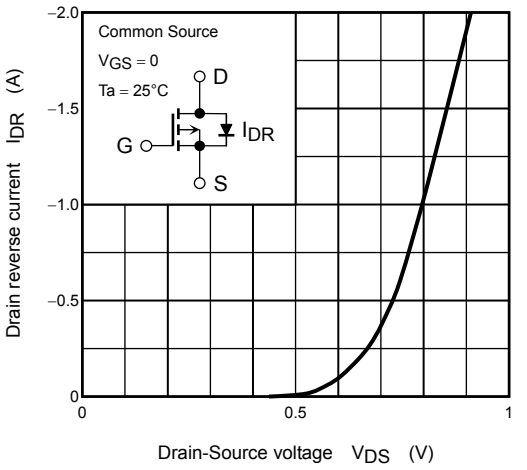
C – V_{DS}



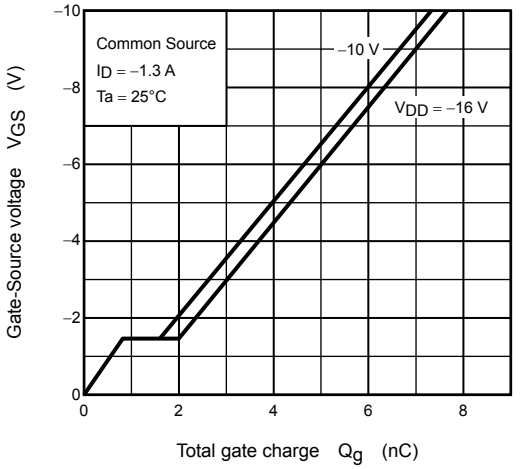
t – I_D



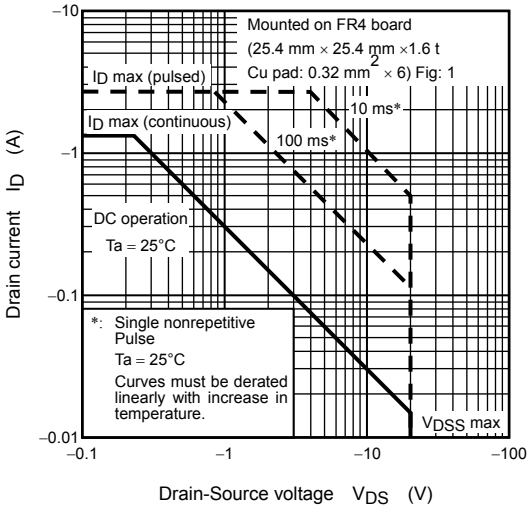
I_{DR} – V_{DS}



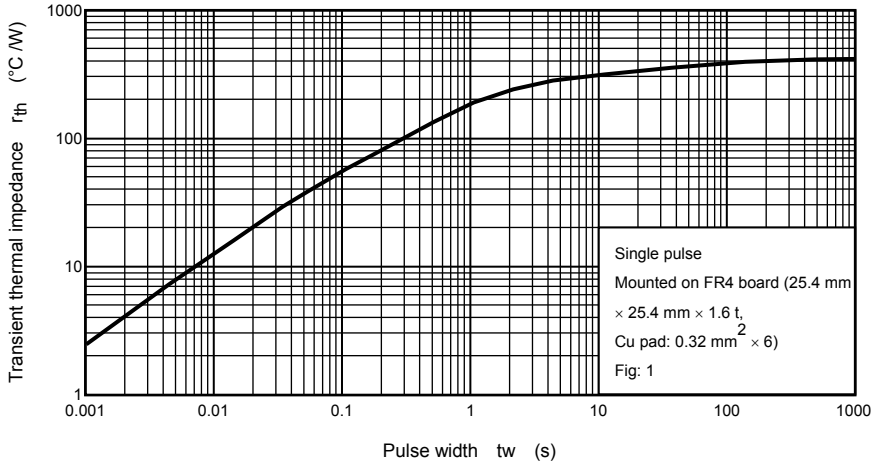
Dynamic Input Characteristic



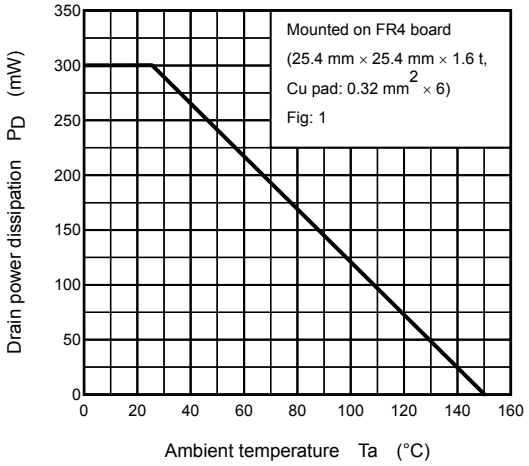
Safe operating area



$r_{th} - t_w$


Transient thermal impedance rth (°C /W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
Single pulse
Mounted on FR4 board (25.4 mm
× 25.4 mm × 1.6 t,
Cu pad: 0.32 mm2 × 6)
Fig: 1

$P_D - Ta$


Drain power dissipation PD (mW)
350
300
250
200
150
100
50
0
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t,
Cu pad: 0.32 mm2 × 6)
Fig: 1

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20070701-EN GENERAL

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